

General Description

It combines planar MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It is suitable for automotive application.

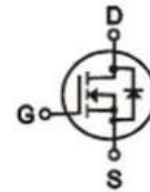
Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

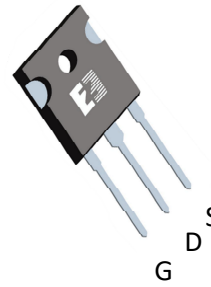
Application

- BLDC Motor driver
- DC-DC
- Load Switch

Product Summary



$V_{DS} = 60V$
 $R_{DS(ON)} = 2.6m\Omega$
 $I_D = 205A$



TO-247



Ordering Information:

Part NO.	ZMPA026N06C
Marking	ZMP026N06
Packing Information	BULK TUBE
Basic ordering unit (pcs)	400

Absolute Maximum Ratings ($T_C=25^\circ C$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	205	A
	I_D	$T_C=75^\circ C$	167	A
	I_D	$T_C=100^\circ C$	145	A
Pulsed Drain Current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$;	820	A
Total Power Dissipation	P_D	$T_C=25^\circ C$	375	W
Total Power Dissipation	P_D	$T_A=25^\circ C$	2.4	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ C$
Storage Temperature	T_{STG}		-55 to +175	$^\circ C$
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, VGS=10V, Rg=25 Ω ,	361	mJ
		L=0.5mH, VGS=10V, Rg=25 Ω ,	650	mJ
ESD Level (HBM)	CLASS 2			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.4	°C/W
Thermal resistance, junction-ambient	$R_{thJA\oplus}$		-	62	°C/W
Soldering temperature (total time<10s)	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=60V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$		2.6	3.3	m Ω
		$V_{GS}=4.5V, I_D=20A$		3.5	4.6	m Ω
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_{SD}=10A$		142		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=20A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	9431	-	pF
Output capacitance	C_{oss}		-	2262	-	
Reverse transfer capacitance	C_{rss}		-	715	-	
Gate Resistance	R_g	$f=1MHz$	-	1.6		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	296	-	nC
Gate - Source charge	Q_{gs}		-	27	-	
Gate - Drain charge	Q_{gd}		-	80	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	17	-	ns
Turn-ON Rise time	t_r		-	80	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	52	-	ns
Turn-Off Fall time	t_f		-	81	-	ns
Reverse Recovery Time	t_{rr}	$V_{DD}=20V, di_S/dt=100A/\mu s, I_S=20A$	-	30	-	ns
Reverse Recovery Charge	Q_{rr}		-	40	-	nC

Fig.1 Gate-Charge Characteristics

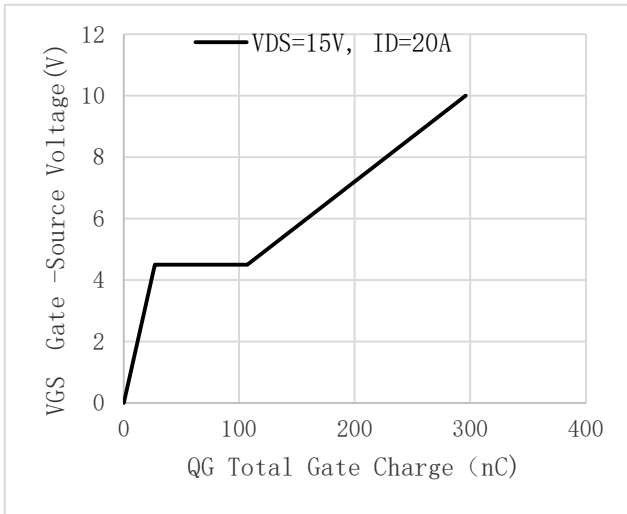


Fig.2 Capacitance Characteristics

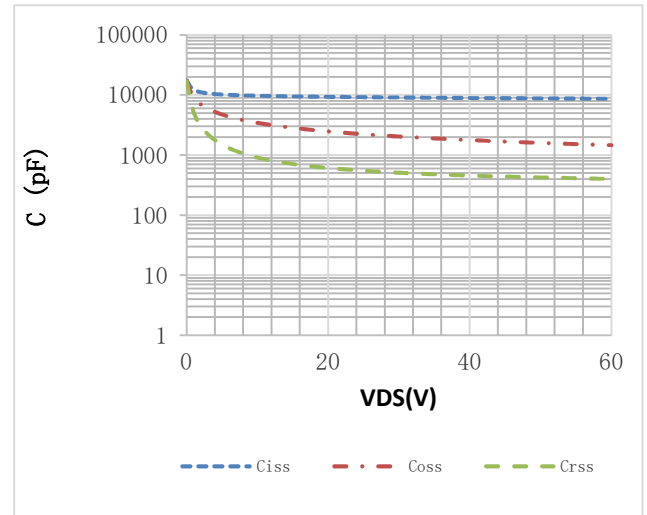


Fig.3 Power Dissipation

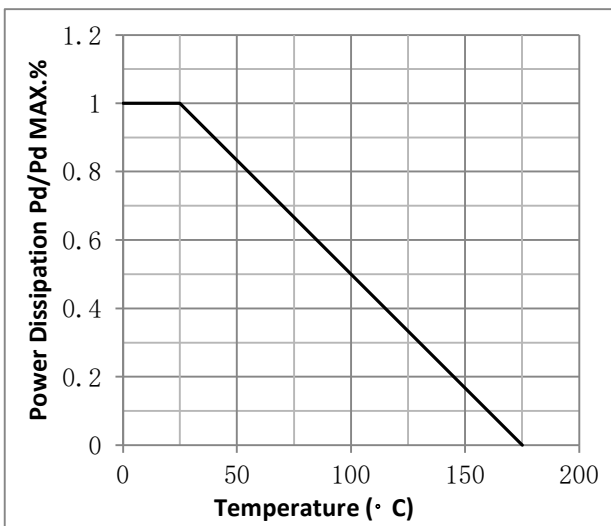


Fig.4 Typical output Characteristics

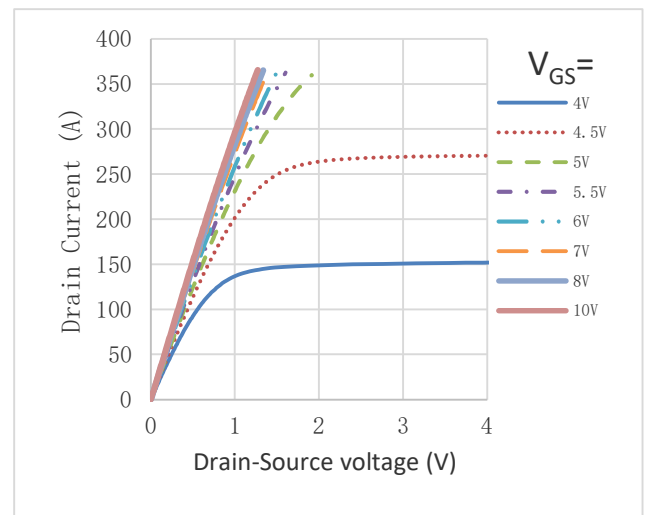


Fig.5 Threshold Voltage V.S Junction Temperature

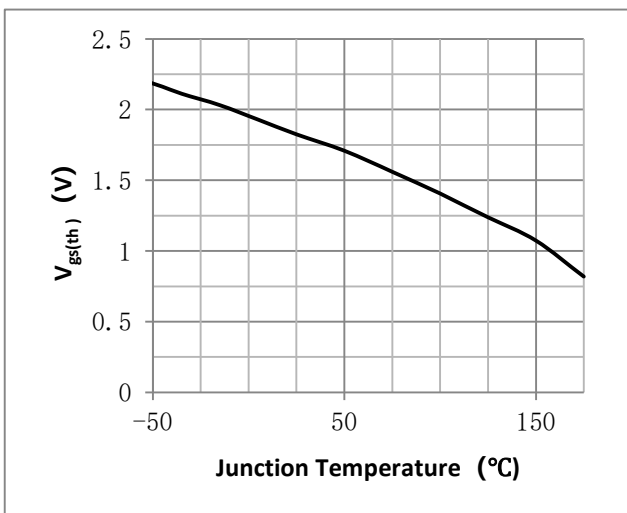


Fig.6 Resistance V.S Drain Current

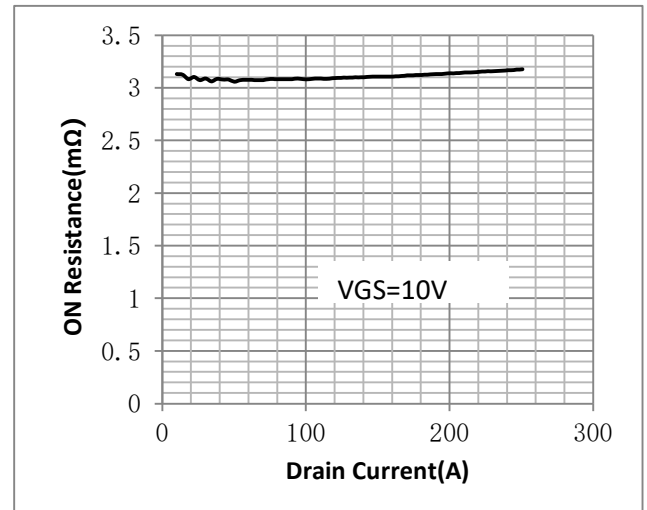


Fig.7 On-Resistance VS Gate Source Voltage

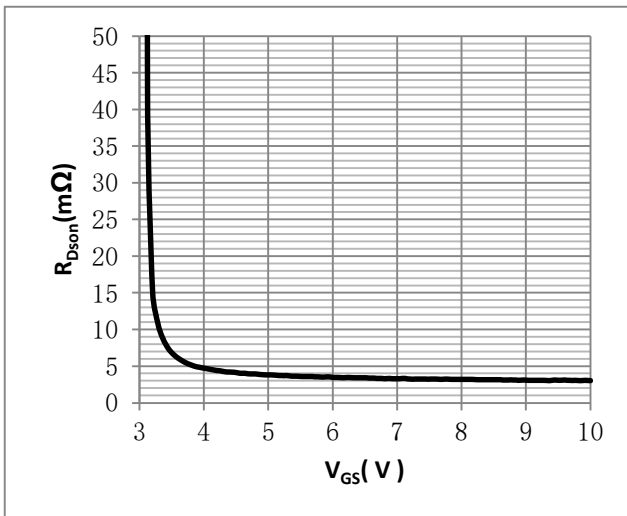


Fig.8 On-Resistance V.S Junction Temperature

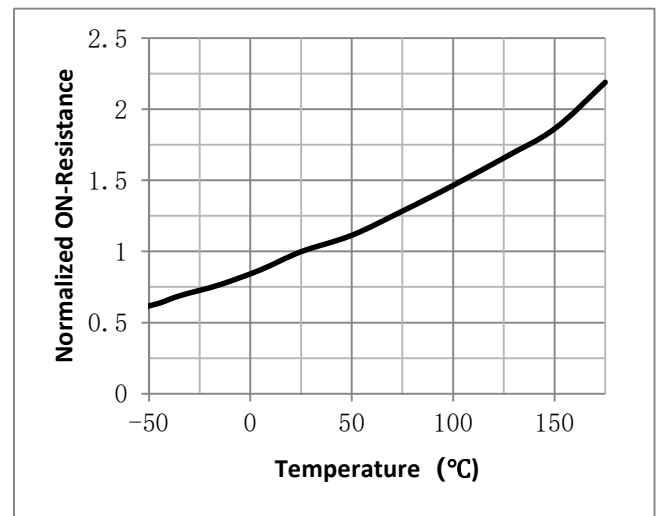


Figure 9. Diode Forward Voltage vs. Current

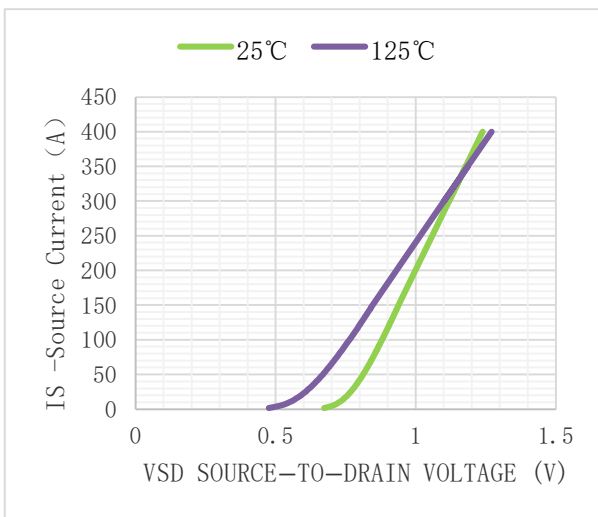


Figure 10. Transfer Characteristics

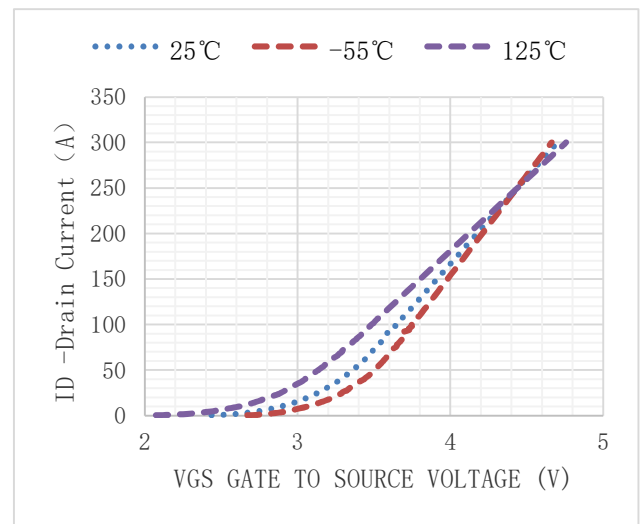


Fig.11 SOA Maximum Safe Operating Area

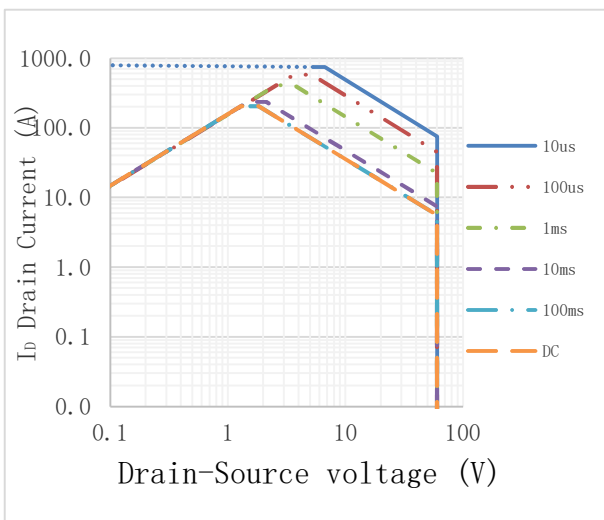
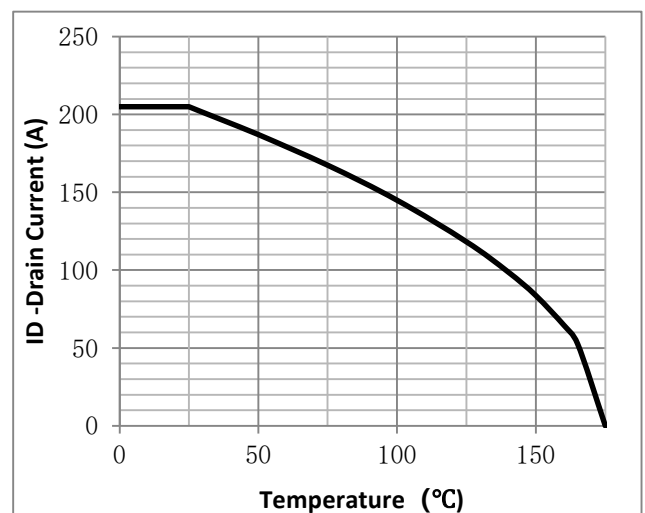
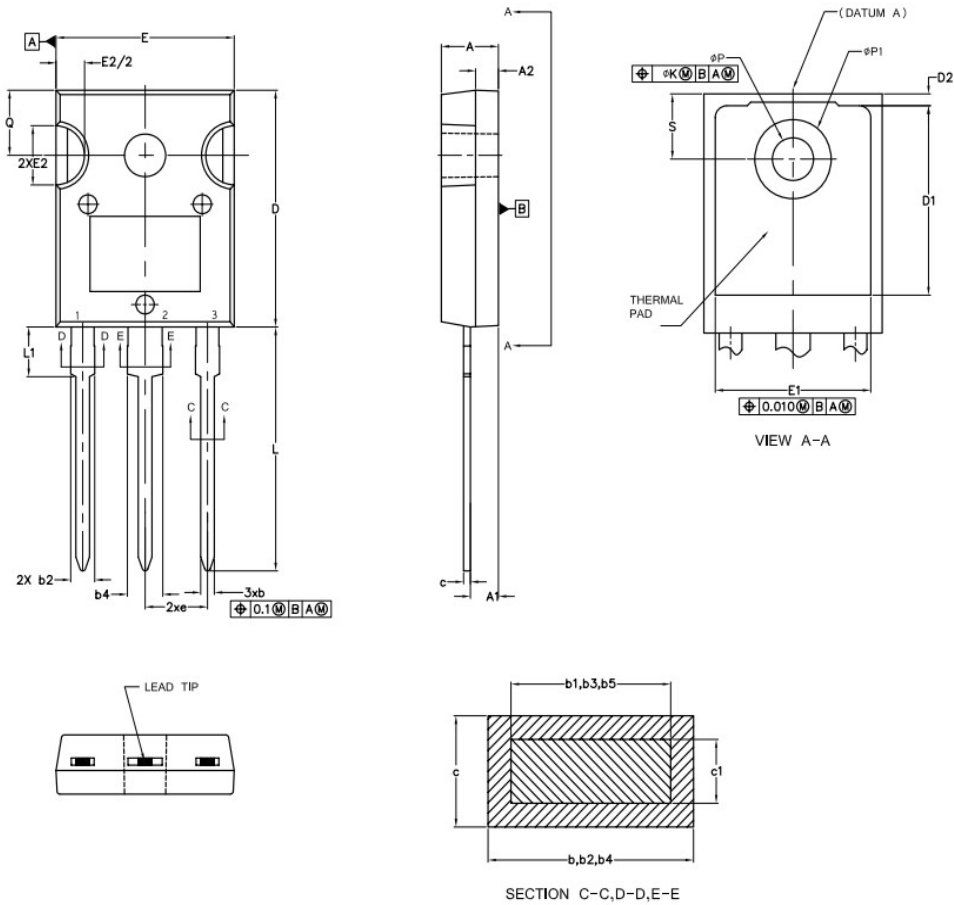


Fig.12 I_D vs. Junction Temperature②



•TO-247 Package Outline



SYMBOLS	DIMENSIONS			
	mm		Inch	
	MIN.	MAX.	MIN.	MAX.
A	4.83	5.13	0.190	0.20
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.65	2.39	0.065	0.094
b3	1.65	2.34	0.065	0.092
b4	2.59	3.43	0.102	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.89	0.015	0.035
c1	0.38	0.84	0.015	0.033
D	19.71	20.70	0.776	0.815
D1	13.08	—	0.515	—
D2	0.51	1.35	0.020	0.053
E	15.29	15.87	0.602	0.625
E1	13.46	—	0.530	—
E2	4.52	5.49	0.178	0.216
e	5.46BSC		0.215BSC	
L	19.57	21.00	0.780	0.827
L1	3.71	4.29	0.146	0.169
φP	3.56	3.66	0.140	0.144
φP1	—	7.39	—	0.291
Q	5.31	5.69	0.209	0.224
S	5.51BSC		0.217BSC	

Note:

- ① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ② Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2024/8/15	New
B	2025/5/24	Correct POD